Synthesizable “Power” – Using Process Portability to Embed PowerPC Cores in Your Chip

Lonn Fiance
Director, Strategic Alliances
Synopsys
Agenda

• Synopsys overview
• PowerPC embedded core overview
• Synopsys’ Synthesizable PowerPC 405/440 offering
• Questions and answers
Global leader in EDA and IP

- Strong global presence:
  - ~4,400 employees, 60+ offices
- Strong technical innovation:
  - 1600+ R&D eng. (~26% of rev.)
- Strong customer support:
  - 1450+ applications engineers

$1.1B revenue in FY04

$285M on R&D in FY04
## Most Trusted in EDA Industry

<table>
<thead>
<tr>
<th>Attribute in selecting vendor</th>
<th>SNPS Rank</th>
<th>Importance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Best after-sales support</td>
<td>1</td>
<td>61%</td>
</tr>
<tr>
<td>Offers competitive prices</td>
<td>3</td>
<td>59%</td>
</tr>
<tr>
<td>Technology leader today</td>
<td>1</td>
<td>46%</td>
</tr>
<tr>
<td>Technology leader in 3 years</td>
<td>1</td>
<td>39%</td>
</tr>
<tr>
<td>Best support of open standards</td>
<td>2</td>
<td>37%</td>
</tr>
<tr>
<td>Best integration w/other tools</td>
<td>2</td>
<td>36%</td>
</tr>
<tr>
<td>Best integration with foundries &amp; IP suppliers</td>
<td>1</td>
<td>35%</td>
</tr>
<tr>
<td>Clear vision of future</td>
<td>1</td>
<td>33%</td>
</tr>
<tr>
<td>Most ethical company</td>
<td>1</td>
<td>32%</td>
</tr>
<tr>
<td>Best documentation</td>
<td>1</td>
<td>28%</td>
</tr>
<tr>
<td>Knowledgeable sales reps</td>
<td>1</td>
<td>24%</td>
</tr>
<tr>
<td>Well-managed company</td>
<td>1</td>
<td>23%</td>
</tr>
<tr>
<td>Best training services</td>
<td>1</td>
<td>23%</td>
</tr>
<tr>
<td>Best before-sales system support</td>
<td>2</td>
<td>12%</td>
</tr>
<tr>
<td>Best Web site</td>
<td>1</td>
<td>7%</td>
</tr>
<tr>
<td>Offers consulting design services</td>
<td>2</td>
<td>7%</td>
</tr>
</tbody>
</table>

**Source:** 2004 EE Times Reader EDA Survey
Need Convergent Optimization Solution
Complete, Correlated And Concurrent

- Design
- IP Reuse
- Verification
- Flows
- DFM
- & Services
Synopsys strategic partnerships assure our customers meet their performance, cost, and schedule goals.
IBM PowerPC® Licensable Cores

**PowerPC 440**

**Key Features**
- 32-bit PowerPC Book E
- Superscalar, 2 inst/cycle
- MMU, 1KB-256MB pages
- 128-bit PLB, 64GB addr

<table>
<thead>
<tr>
<th>Feature</th>
<th>440</th>
<th>440-S</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>2.5mW/MHz</td>
<td>1.5mW/MHz</td>
</tr>
<tr>
<td>Tech</td>
<td>32K/32K 0.18um 15.5mm²</td>
<td>32K/32K 130nm 9.8mm²</td>
</tr>
<tr>
<td>Fully Synthesizable</td>
<td></td>
<td>32K/32K Fully Synthesizable</td>
</tr>
</tbody>
</table>

**PowerPC 405**

**Key Features**
- 32-bit PowerPC Embedded
- Scalar, 1 inst/cycle
- MMU, 1KB-16MB pages
- 64-bit PLB, 4GB addr

<table>
<thead>
<tr>
<th>Feature</th>
<th>405</th>
<th>405-S</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>1.9mW/MHz</td>
<td>0.9mW/MHz</td>
</tr>
<tr>
<td>Tech</td>
<td>16K/16K 0.18um 8.0mm²</td>
<td>16K/16K 130nm 3.8mm²</td>
</tr>
<tr>
<td>Fully Synthesizable</td>
<td></td>
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</tbody>
</table>
## PowerPC 405 Features

<table>
<thead>
<tr>
<th>Architecture</th>
<th>32-bit PowerPC Embedded Application code compatible with all PowerPC microprocessors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Special Features</td>
<td>Hardware multiply / divide 24 DSP instructions (16x16+32) 32-bit x 32 general purpose registers</td>
</tr>
<tr>
<td>CPU Pipeline</td>
<td>5 Stage Pipeline Single instruction per cycle</td>
</tr>
<tr>
<td>Caches</td>
<td>16KB, 2-way set associative, 32-byte line, no locking, parity</td>
</tr>
<tr>
<td>MMU</td>
<td>64 entry UTLB – full associatitivity 4 entry ITLB, 8 entry DTLB 5 cycle miss penalty Variable pages – 1KB to 16MB</td>
</tr>
<tr>
<td>Branch Pred.</td>
<td>Static</td>
</tr>
<tr>
<td>Physical Address</td>
<td>32-bit (4GB physical address) 64- or 128-bit interface to Processor Local Bus (PLB) On-chip memory supported via PLB</td>
</tr>
<tr>
<td>Debug</td>
<td>JTAG and Trace FIFO ports Real-time, non-invasive trace supported</td>
</tr>
</tbody>
</table>
# PowerPC 440 Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>Architecture</td>
<td>32-bit PowerPC Book E Application code compatible with all PowerPC microprocessors</td>
</tr>
<tr>
<td>CPU Pipeline</td>
<td>Two-way superscalar 7 Stages, out of order issue, execution and completion</td>
</tr>
<tr>
<td>L1 Caches</td>
<td>32KB, 64-way set associative, transient and locked cache region mechanism, software managed coherency, parity</td>
</tr>
<tr>
<td>MMU</td>
<td>64 entry UTLB – full associativity 4 entry ITLB, 8 entry DTLB 3 cycle ITLB/DTLB miss penalty</td>
</tr>
<tr>
<td>Branch Pred.</td>
<td>Dynamic 16-entry BTAC, 4K-entry BHT</td>
</tr>
<tr>
<td>Physical Addr</td>
<td>36-bit (64GB physical address)</td>
</tr>
<tr>
<td>Core Interfaces</td>
<td>Three independent 128-bit PLB4 master ports (instruction read, data read, data write), each with separate address bus</td>
</tr>
<tr>
<td>Debug</td>
<td>JTAG and Trace FIFO ports Real-time, non-invasive trace supported</td>
</tr>
</tbody>
</table>
The Power of Flexibility

• Each application has unique requirements
  - **Business**: cost, delivery time, existing supplier relationships, design services, etc.
  - **Technical**: process technology, integration, packaging, performance, other IP, etc.
  - **Life cycle**: process migration, multi-sourcing, cost reductions, strategic options

• Process portability provides flexibility to address these requirements

• Flexibility is key to proliferation
Flexibility Creates Value

- Design Value is a complicated function
  \[ \text{Value} = f(\text{Area, Performance, Power, Yield, IP, Packaging, Process, Delivery Time, Reliability, Risk, Location}) \]
- Complex interaction between the parameters
- Intelligent tradeoffs increase value
  - Design specific

Example Trade-Offs

![Performance vs. Area or Power graph](graph.png)
PowerPC 405-S & 440-S Overview

• **Macro Objective:**
  - Technology independent, reusable and fully synthesizable PowerPC cores

• **Design Objectives**
  - Standard SRAM’s and Register Files for Caches and UTLB’s
  - Maintain cycle compatibility with the existing PowerPC 4xx
  - Target performance of 300 MHz (440-S) and 250 MHz (405-S) for Artisan TSMC 13 LVFSG
  - Fault coverage goal of >98%
  - Use a complete Synopsys tool flow

• **Verification Objectives**
  - Create a portable verification environment
  - Create tests to verify the major architectural capabilities

• **Easy delivery and use via Synopsys DesignWare**
Synopsys Power Solution - Design Flexibility and Portability

• System C models
  ▪ System-level SystemC models
  ▪ Instrumented for System Studio

• SoC Design
  ▪ Design View
  ▪ Implementation View
  ▪ CPU, SoC testbenches with test suites

• Documentation
  ▪ Implementation scripts with README’s
  ▪ User Guide, Data Book, App Notes, etc.

• Support
  ▪ Award-winning customer support
  ▪ Qualified design services and complimentary IP
SystemC Models

• C++ class library to model SoC hardware and processes
• Used for system-level design
  ▪ Architectural analysis of processors, buses, custom logic, and IP
• Explore hardware/software tradeoffs
• SystemC is an open industry standard
  ▪ Tool and IP support from multiple companies
• C++ basis allows concurrent development of hardware and software
Synopsys SystemC Deliverables

• Original models, testing and validation from IBM
• Synopsys distributes and supports
• Instrumented for System Studio

SystemC Model List
• PowerPC 405 Processor Core
• PowerPC 440 Processor Core
• PLB4 (Processor Local Bus v4.x)
• DMA Controller (PLB4)
• DCR (Device Control Register)
• UIC (Universal Interrupt Controller)
• UART (Universal Asynchronous Receiver Transmitter)
• MCMAL PLB4 (Multi-channel Memory Access Layer)
• Memory (DDR) Controller (PLB4)
• EBC (External Bus Controller)
• OPB (On Chip Peripheral Bus)
• PLB4 to OPB Bridge
• OPB to PLB4 Bridge
• PCI-X to PLB4
• PCI-Express
Design View coreKit Overview

- "Black Box" Verilog Models for the PowerPC 4xx-S
  - Fixed configuration to determine feasibility
  - Cycle compatible VMC model of the 4xx-S
  - VERA based CPU testbench
  - Timing model for WC operating conditions for Artisan TSMC 13 LVFSG
  - All appropriate documentation (databook, datasheet, etc.)

- PLB-to-AHB Bridge Verilog Model
  - Cycle compatible VMC model of the PLB2AHB Bridge
  - VERA based SOC testbench for the PLB2AHB Bridge
  - Application note

- Available to DesignWare licensees at no additional charge
Testbench - 440-S CPU
These IP’s are not delivered as a part of the core kit, but has to be installed separately. However the testbench will be instantiating these components.
Implementation View coreKit Overview

• RTL source for PowerPC core and PLB-to-AHB Bridge
  ▪ Configurable via coreAssembler
  ▪ Portable RTL validated by both IBM and Synopsys

• Implementation scripts with documentation
  ▪ RTL simulation in an automated verification environment
  ▪ Default floor plans
  ▪ Integration of technology specific RAMs
  ▪ Logical and physical synthesis with clock tree synthesis
  ▪ Scan insertion and ATPG
  ▪ Formal verification
  ▪ Power optimization and analysis
    ➢ Complete RTL-to-GDSII capability

• Documentation for SoC integration
  ▪ User Guide, Data Book
  ▪ App Notes

• Licensing
  ▪ PowerPC license from IBM
  ▪ DesignWare license from Synopsys
**Design View Flow**

1. Install Design View coreKit
2. Create coreConsultant workspace
3. Install VMC Model
4. Simulate VMC Model in standalone verification environment
5. Simulate VMC Model in application verification environment
6. Synthesize application logic using PowerPC 4xx Star IP CPU’s timing model to check approximate timing
7. Get Implementation View coreKit

**Implementation View Flow**

1. Install Implementation View coreKit
2. Create coreConsultant workspace
3. Configure RTL
4. Simulate configured RTL in standalone verification environment
5. Simulate configured RTL in application verification environment
6. Integrate technology specific RAMs
7. Synthesize (RTL-to-gates)
8. Insert scan
9. Create floorplan
10. Run physical synthesis
11. Create test vectors
12. Run STA
13. Formally verify gate-level netlist
14. Simulate gate-level netlist
15. Perform power analysis
## Synopsys Tool Support in coreKit

<table>
<thead>
<tr>
<th>Product</th>
<th>Capability</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCS®</td>
<td>RTL simulation</td>
</tr>
<tr>
<td>Vera</td>
<td>Verification Testbench</td>
</tr>
<tr>
<td>Design Compiler®</td>
<td>Logic synthesis</td>
</tr>
<tr>
<td>Physical Compiler®</td>
<td>Physical synthesis</td>
</tr>
<tr>
<td>JupiterXT™</td>
<td>Design planning</td>
</tr>
<tr>
<td>Astro™</td>
<td>CTS scripts for detailed placement and routing</td>
</tr>
<tr>
<td>DFT Compiler</td>
<td>Design-for-test insertion</td>
</tr>
<tr>
<td>TetraMAX®</td>
<td>Test pattern generation</td>
</tr>
<tr>
<td>DesignWare BIST</td>
<td>Built-In-Self-Test capability</td>
</tr>
<tr>
<td>Power Compiler™</td>
<td>Power optimization</td>
</tr>
<tr>
<td>PrimePower</td>
<td>Full-chip power analysis</td>
</tr>
</tbody>
</table>

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Default IBM PowerPC 440-S Floorplan

128-bit Processor Local Bus

- 32KB I-cache w/parity
- 32KB D-cache w/parity

- MMU
- Instruction Unit
- Branch Unit
- Complex Integer Pipe
- Simple Integer Pipe
- Load / Store Pipe
- MAC
- Timers
- Power Management
- Debug/Trace
- Interrupts

PowerPC 440 Core

Diagram showing the layout of the PowerPC 440-S floorplan with various components such as DCA, ICA, UTLB, I-cache, D-cache, Control, MMU, Pipe, Complex Integer Pipe, Simple Integer Pipe, Load / Store Pipe, MAC, Timers, Power Management, Debug/Trace, and Interrupts.
Default IBM PowerPC 405-S Floorplan
Synopsys DesignWare® IP portfolio

DesignWare Star IP
DesignWare Library
DesignWare Cores
DesignWare Verification Library

Microprocessor cores from leading Star IP providers
Infrastructure IP, including high-speed datapath generators
Portfolio of digital and analog connectivity IP
Simulation models of buses & I/O standards
Benefits for PowerPC in DesignWare

- **Broad Availability**
  - 25,000+ DesignWare users worldwide

- **Availability of supporting IP components**
  - Fully Integrated with AMBA™ peripherals
    - AMBA AHB/APB w/ automated subsystem assembly
    - All DesignWare peripherals supported
  - Native CoreConnect™ interface retained and supported

- **Industry recognized first-tier customer support**
  - Experienced technical support infrastructure

- **Tested with complete design flow**
Summary

• All program objectives achieved
  ▪ Cycle compatibility with existing 440 and 405 cores
  ▪ Single cycle cache access
  ▪ Target performance of 300 MHz (440-S) and 250 MHz (405-S) achieved
  ▪ Portable verification environment and critical test cases packaged in core delivery

• Synopsys is a “one-stop shop” for synthesizable PowerPC 440 and 405 cores
  ▪ Complete tool flow from RTL to CTS
  ▪ Knowledge of CoreConnect and AMBA peripherals
  ▪ Supported through DesignWare
  ▪ Synopsys Professional Services are experts in PowerPC core and system implementations
Synopsys and Power
A Complete and Flexible Solution

Partners
- IBM
- Power.org
- Foundries

Services
- PowerPC experience
- Low power, SoC design
- Complete Flow Expertise

IP
- Distribution & support (DesignWare)
- Proven Reusability Methodology
- #1 Connectivity IP provider
- Core Connect and AMBA IP

Tools
- System-Level Design Capability
- Complete Functional Verification
- Complete PowerPC and SoC Implementation Flow
- Post GDS Solution (OPC, PSM, fracturing)